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EXAMINER
SOUW, BERNARD E

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 05/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/583,617	GORUGANTHU ET AL.	
	Examiner	Art Unit	
	Bernard E Souw	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The Amendment B, filed on 03/31/2003, Paper No.6/B, in response to the second Office Action dated 12/16/2002 has been entered.

▶ New claims 24-29 have been added.

▶ Claim 20 has been previously cancelled per Amendment A, filed 12/05/2002, paper no.4/A.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Finality of Previous Office Action Withdrawn

3. The Finality of the previous Office Action (dated12/16/2002, paper no.5) is withdrawn, because the Examiner has a new & different interpretation of Applicant's response to the previous § 112 rejections of claims 1 and 16 (and the cancelled claim 20). This withdrawal of finality is ***NOT*** because "*the examiner introduced a new ground of rejection in connection with the Section 103(a) rejection, effectively repeated grounds of rejection for various claims and failed to respond to Applicant's previous arguments regarding these repeated issues*", as alleged by Applicant in his Response to Final Office Action, paper no.6/B.

In the contrary, there is ***no*** new ground of rejection raised in the previous Office Action, except those solely caused by Applicant's response to a previous § 112 rejections of claims 1, 16 and 20. As will be clear in the following sections, all the grounds of rejections are proper (although now applied in a different mode, i.e., *simultaneously* instead of *alternatively*, but both *unchanged*), and are thus repeated without any change in this new Final Office Action. As also will be clear in the following sections, all previous rejections do not fail, as alleged by Applicant, and are therefore repeated in their original form, with emphasis where needed.

Previous 35 USC § 112 Rejections Withdrawn

4. The previous § 112 second paragraph rejections of claims 1, 16 and 20 are withdrawn because of Examiner's new & different interpretation of Applicant's response (paper no.4/A) upon Examiner's question raised in the first Office Action, i.e., whether the "*region of the insulator of the SOI structure*" is the same as "*a BOX portion of the SOI structure*", as recited in the first Office Action (paper no.3, pg.2/lines 8-10 from bottom), and once again in the second Office Action (paper no.5, pg.2/lines 7-9). Applicant's response, as stated in paper no.4/A, page 2, lines 9-11, recites, "*while it (BOX) can be used to refer to a type of insulator (i.e., oxide insulator) in an SOI structure, this term (BOX) does not necessarily connote an SOI structure since it may also be used in a non-SOI structure*". This dubious interpretation is confirmed by Applicant in his second response (paper no.6/B) on pg.6/lines7-9 from bottom, reciting

"*Therefore, while the insulator portion of the SOI structure may include buried oxide (BOX), it is not limited to BOX*".

In both previous Office Actions, such an *inconclusive* or *dubious* response has been interpreted by the Examiner in the alternative mode, i.e., in an *either-or* sense. Such interpretation has previously led to using Yoshida's Fig.5 as a prior art to reject claim 1, i.e., by assuming the exposed "*insulator of the SOI structure*" recited in claim 1 as being the (part of) SOI under the gate layer between source (S) and drain (D), while in the alternative, using Yoshida's Fig.1 to reject claim 16, i.e., by interpreting the exposed "*insulator of the SOI structure*" recited in claim 16 as being the BOX layer.

Note, **both** interpretations, **either** as *insulator portion of SOI* between S and D (Fig.5) **or** as a *BOX* layer (Fig.1) are already applied by the examiner since the first Office Action, although in an ***alternative*** manner, and ***not in a simultaneous*** manner. Because of Applicant's *inconclusive* or *dubious* response, as stated above, the Examiner in the second Office Action has (mistakenly) decided to *drop off the first interpretation* (SOI insulating portion between S & D) and *exclusively use the second interpretation* to ***both*** claims 1 and 16. This mistake is the ***only mistake*** to be corrected in this new Office Action, and thus represents the ***only ground*** for the above Finality Withdrawal.

In the present Office Action, Applicant's *inconclusive* or *dubious* response, as stated above, is interpreted in a *simultaneous* manner, i.e., the "insulator" of claims 1 and 16 (claim 20 is cancelled) being interpreted as *both* the (insulating part of the) SOI, thus referring to Yoshida's Fig.5, and *also* as a BOX layer, thus referring to Yoshida's

Fig.1. Since such simultaneous function is, of course, impossible, the new rejection of claims 1 and 16 are presented twice, first as the (insulating part of the) SOI (Yoshida's Fig.5) and then as a BOX layer (Yoshida's Fig.5). These two grounds of rejection are considered together to simultaneously reject Applicant's *inconclusive* or *dubious* interpretation of the exposed "insulator" in claims 1 and 16.

Note, the *two* grounds of rejection *both have been already applied* in the first Office Action in an *alternative* manner. Consequently, the present ground of rejection is *not* a *new* ground of rejection. Similarly, the previous decision made in the *second* Office Action, i.e., dropping off the (insulator part of) SOI interpretation while retaining only the BOX interpretation, can *not* be regarded as a *new* ground of rejection, as alleged by Applicant, since both grounds are *have been already* applied in the *preceding*, i.e., the *first*, Office Action.

Therefore, Applicant's repeated allegation of a *new ground of rejections* made by the Examiner is completely groundless, and is herewith rejected.

Examiner's Response to Applicant's Arguments (Paper No. 6/B)

5. Applicant's argument in paper no.6/B, pg.6/lines 11-13, allegedly that "*the Examiner has incorrectly asserted that 'while BOX and SOI are both insulators, the SOI can be turned into active semiconductor layers'* ", has been taken out of context by the Applicant, noting thereby that what the Examiner meant is quite understandable to anyone of ordinary skill in the art. In that sentence quoted by the Applicant, the SOI is to be interpreted in context of the *directly preceding sentence*, also quoted by the

Applicant on the same page, line 14, i.e., "*the insulator of the SOI structure*". It is silly to interpret the Examiner's sentence such as what the Applicant has done, since it is well known in the art that SOI is a structure, containing both insulators and conductors. That '*SOI can be turned into active semiconductor layers*', is also a fact well known in the art. Thus, none of Applicant's allegations are correct and acceptable.

6. Applicant's further argument in paper no.6/B, pg.6/lines 10-11, *allegedly refuting* Applicant's "*confusion*" between "*insulator portion of SOI*" and "*BOX*" while insisting that the two are *not the same*, as recited in Applicant's own words, "*This assertion is incorrect (?), as discussed in the previous traversal (repeated above), SOI and BOX are not the same*" (the question mark and the underlines added for emphasis), is based on a grave misunderstanding and also self-contradictive, since Applicant's statement can only mean that Applicant principally agrees with the Examiner in that the two are different and they have to be distinguished one from the other, exactly as insisted by the Examiner in the first and second Office Actions.

7. Canceling a claim and then arguing about specific words used in the cancelled claim, as recited by Applicant in paper no.6/B on pg.7/lines 11-13, is a dirty trick that is to be strongly objected. The word BOX has been used in claim 20, which has been cancelled. A distinction of BOX and (insulting portion of) SOI was necessary in order to decide between using Yoshida's Fig.1 or Fig.5 as prior art to reject claims 1 and 16. Applicant's *inconclusive* or *dubious* response (using the wording, "*can be used ... does not necessarily*") is here a solid and undeniable evidence that such a distinction would

have been necessary in rejecting claims 1 and 16, even if the word "BOX" is not explicitly recited, since Applicant's would allow both interpretations, (insulator of the) SOI, as well as BOX. Thus, the word "BOX" remains an issue for claims 1 and 16. *Consequently, the previous § 112(2) rejection of claims 1 and 16 was proper* under the *either-or* interpretation of the words "*insulator of the SOI structure*" in claims 1 and 16, as stated above.

However, this previous § 112(2) rejection of claims 1 and 16 is now withdrawn because of a new interpretation of the words "*insulator of the SOI structure*". Note, what is new is only the *Examiner's decision*, how to interpret the words "*insulator of the SOI structure*", both alternative interpretations having been *already made since the first Office Action*. Moreover, and most importantly, *no new ground of rejection* is raised by the Examiner, since *both* interpretations have been already applied since the first Office Action. *Therefore, the Finality of the previous Office Action was proper*. As unambiguously stated above, the present withdrawal of the previous Finality is based on a fully different reason.

8. Regarding Applicant's arguments on pg.6/lines 10-11, requesting clarification of the Examiner's statement that "*claims 1-14, 16-19 and 21-23 stand rejected under 35 U.S.C. §102(a) and 102(e)*", there is no explanation necessary, since the word *and* can not be misunderstood by anyone who has a proper understanding of the English language. Also, the statute for each rejection is clearly stated: A §102(a) rejection is based on a publication as prior art, whereas a §102(e) rejection is based on a patent (or patent application) as prior art. In the present case, Yoshida's is a patent, which is

judicially also valid as a publication. Therefore, Yoshida's are valid as prior art for both 35 U.S.C. §102(a) *and* §102(e) rejections. In this case, the Applicant as well as the Applicant Attorney(s) certainly would not disagree with the Examiner that a *double rejection* is *better* than a *single rejection*.

9. Regarding Applicant's argument that Examiner's §102 rejection of claim 3 is improper, it is to be emphasized that the limitation "*detecting secondary electrons wherein analyzing the die includes a scanning electron microscope (SEM)*" is *inherent* to Yoshida's, thus rendering the previous §102 rejection totally *proper*. As generally known in the art, a scanning electron microscope is *any* device that is capable of performing the following functions, (a) electron beam (EB) irradiation, (b) detecting secondary electrons generated by the EB on the sample, (c) scanning the EB to generate an image, (d) having resolution capability of microscopic scale (e.g., transistor details), and additionally, although not critical as criterion but only emphasizing the function of a conventional microscope, (e) an image-magnifying capability. Functions (a)-(d) is inherent in Yoshida's, as recited in Col.5/ll.42-46, Col.5/ll.53-60 and Col.6/ll.7-11, referring to Fig. 2 and Fig.13, whereas function (d) is also inherent in Yoshida's, as recited in Col.10/claims 2, 6, 8 and 10. Specifically, Yoshida's EB source 13, the EB 15, sample 1X, secondary electrons 16 and secondary electron detector 14, in combination with Yoshida's claims 2, 6, 8 and 10, effectively form a secondary electron microscope as recited in Applicant's claim 3.

Therefore, against Applicant's mistaken allegation, the previous §102 rejection of claim 3 is ***proper***, because a *modification of the sole/primary reference by a secondary*

*prior art is **not at all** necessary.* Thus, the Official Notice taken by Applicant in the first and second Office Actions is now taken back by the Examiner, and ***all*** supporting prior arts are eliminated in the present §102 rejection of claim 3.

Since additional prior arts have been readily recited in *both previous* Office Actions, they again will be presented in this Office Action in an *additional* rejection under 35 U.S.C. §103(a) of claim 3, as being obvious over a *single prior art* (Yoshida's) with an Official Notice supported by *the already recited* prior arts.

10. Regarding Applicant's argument that the previous §102 rejection of claim 7 is improper, it is to be emphasized that a power supply is inherent in Yoshida's testing set 11, as recited in Col.5/ll.53-55. Applicant's claim that Yoshida's device does not include a power supply is an obvious violation of natural law, since no device could operate without power input. *Therefore, a power supply must be inherent to Yoshida's, thus rendering the previous §102 rejection of claim 7 proper.*

11. Regarding Applicant's argument that Examiner's §102 rejection of claim 13 is improper, it is to be emphasized that the limitation "*inputting signals known to induce a failure*" which is interpreted by the Examiner as being the same as "*inputting a signal (that is varied) until a failure is induced in the die*", is a *mere matter of deliberate choice that is already inherent* in Yoshida's use of DUT (device under testing) board 12, as already recited in the previous Office Actions. For example, inputting a signal pulse of 10 kV through Yoshida's DUT is *inherently* understood (***i.e., known***) to cause a certain

failure in the die. *Therefore, the previous rejection of claim 13 is proper*. (An *additional* § 103(a) rejection of claim 13 is also provided in this Office Action).

Regarding Applicant's argument that claim 13 is *not directed* to "*either the use of a DUT board or stimulating a response until failure is induced in the die*", it is to be emphasized that Yoshida's (use of) *DUT board is capable* of performing what *Applicant intends to do*. In particular, a recitation of the intended use of the claimed invention, in this case the method of "*inputting signals to induce a failure*" as claimed in claim 13 (dependent on claim 12 dependent on claim 11, which finally depends on the method of analyzing a semiconductor die according to claim 1) must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior arts, i.e., Yoshida's (use of) DUT board. If the prior art structure (Yoshida's DUT board) is capable of performing the intended use (*inputting signals to induce a failure*), *then it meets the claim*. *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Still regarding Applicant's argument that claim 13 is *not directed* to "*either the use of a DUT board or stimulating a response until failure is induced in the die*", it is noted that such a limitation is not recited in claim 13. In this respect, the limitations of claim 13 are regarded as self-sufficient steps of a method, including the limitations of parent claims 12, 11 and 1. Neither specific device structures nor method steps are found as examples or embodiments in the specification. They were neither explicitly found in the claims, nor were the words that are used in the claims so defined in the specification to require limitations prohibiting the use of Yoshida's DUT board. A reading of the

specification provides no evidence to indicate that these (negative) limitations must be imported into the claims to give meaning to disputed terms. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

12. Regarding Applicant's argument that Examiner's *alternative §103 rejection* of claim 14 is improper, for allegedly failing to give *an evidence of motivation* for the step of inputting a signal in a continuous loop as an automation of a step or method which is normally implemented manually. A motivation, as well as an evidence for motivation (i.e., in form of an auxiliary teaching), is here not necessary, since the step is conventional and also well known in the art, while also involving only routine skill in the art. In such a case, the rationale to modify the prior art Yoshida, i.e., to input a signal in a continuous loop as an automation of a step or method, instead of inputting such a signal manually, does not have to be expressly stated in the prior arts; in the present case the rationale is reasoned from knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

This relates to suggestion/motivation in that "having established that this knowledge was in the art, the Examiner could then properly rely on a conclusion of obviousness 'from common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular reference'." *In re Bozek*, 416 F.2d 1385, 1390, 163 USPQ 545, 549 (CCPA 1969).

For the reasons stated above, the previous *alternative §103 rejection* of claim 14 is thus *proper*. In this Office Action, the *previously alternative §103 rejection* is

presented as a principal ground of rejection of claim 14, i.e., eliminating the previous §102 rejection. Furthermore, a motivation is provided, although it is not necessary.

13. Regarding Applicant's argument that the previous §102 rejections of claims 16 and 17 are improper, it is to be emphasized that the limitation of a detector is inherent in Yoshida's. A detector is recited in Col.5/line 57 and Col.6/line 14, whereas an imaging device, which is also a detector, is recited in Col.5/ll.58-59 and Col.6/line 52. No modification of Yoshida's is necessary, and therefore, *the previous §102 rejections of claims 16 and 17 are proper*.

14. Regarding Applicant's argument that Examiner's §102 rejection of claim 22 is improper, it is to be emphasized that the limitation "*image of the die having light and dark areas*", *the white portions having a lower potential than the black portions*, is recited by Yoshida in Col.6/ll.1-4. *Therefore, the previous §102 rejection of claim 22 is* ***proper****, because a modification of Yoshida's is not at all necessary.* An Official Notice as given in the first and second Office Actions is not at all necessary, and is therefore omitted by the Examiner in the present Office Action.

15. The following section clarifies Applicant's allegations that the previous Office Action have failed to respond to Applicant's previous arguments, by pointing out explicitly, that response has been made to each of Applicant's previous arguments.

Response to Applicant's Previous Arguments (Paper No. 4/A)

16. Applicant's argument in paper no.4/A, page 2, lines 9-10, that the previous §102 rejections of claims 1, 16 and 17 have failed to teach "*inducing a detectable response from the exposed region of the insulator*", is herewith rejected, because the Examiner's has evidently responded to that issues in the 1st Office Action (pg.4, lines 3-4) by reciting Yoshida's Col.6/ll.46-57, (additionally by Col.6/ll.57-63), and in the 2nd Office Action (page 5/lines 9-11) by reciting Yoshida's Col.5/ll.19-32 and ll.52-60.

17. Regarding Applicant's further argument on page 3, lines 1-5, reciting that "*inducing a detectable response from the exposed region*" is not taught by Yoshida, allegedly since the insulating layer 1c in Fig.5 is removed, it is to be emphasized that *an absence of secondary electrons is also a detectable response*, since here "*detectable*" means "*distinguishable*" as compared to the signals from neighboring areas, whereas "*response*" can be either positive (measurable secondary electrons) or negative (no secondary electrons). That an absence of secondary electrons is still to be considered as a detectable signal, has been already pointed out with regard of the rejection of claim 9 in both previous Office Actions.

18. Therefore, based on the above evidence of Examiner's existing response, *Applicant's traversal* of the Finality of the previous Office Action based on Examiner's alleged negligence of not responding to *all* Applicant's arguments, *is herewith strongly rejected*, for being based on unfounded allegations and false accusations.

19. For all the reasons stated above, all the previous §102 and §103 rejections are repeated below in its original forms (as directly adopted from previous 1st and 2nd Office Actions without editing), plus some emphasizing phrases that are underlined, as proof that no new ground of rejection is thereby raised. However, in addition to these repeats, new additional rejections of some claims are also being provided. These additional rejections are to be considered as a reinforcement of the existing, unchanged grounds of rejections, since --*as the Applicant, as well as the Applicant's Attorney(s), certainly would not disagree*-- double rejections are always better, especially in the present particular case.

Claim Rejections - 35 USC § 112

20. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 28 and 29 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 28 and 29 recite the limitations of "*(detecting) logic states*" and "*(plurality of) circuit nodes*", both of which are not described in the specification.

Claim Rejections - 35 USC § 102

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 2, 8-11, and 16-19 stand rejected under 35 U.S.C. §102(a) and §102(e) as being *clearly anticipated* by Yoshida (USPAT #6,137,295).

22. Regarding claims 1 and 16, *in the event that Applicant interprets the "insulator of SOI structure" recited in claims 1 and 2 as a BOX layer*, as previously raised in the second Office Action, Yoshida invents a method for analyzing a semiconductor die (2, 3) having silicon-on-insulator (SOI) structure 1s and a back side opposite circuitry 1f & 1g near a circuit side, as shown in Fig.5, the method comprising:

- removing substrate 1a shown in Fig.5 from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure (the section between the two diffusion regions on the left of the exposed region 1j) where the substrate (1a) has been removed (1j), as recited in Col.6/ll.46-57; and

- inducing a detectable response from the exposed region as a function of a portion of the circuitry, as recited in Col.6/ll.51-57. and therefrom, analyzing the die, as recited in Col.5/ll.19-32.

This ground of rejection is the same as previously made in the 1st Office Action.

23. Still regarding claims 1 and 16, *in the event Applicant interprets the "insulator of SOI structure" recited in claims 1 and 16 as the insulator layer beneath the gate between the S & D layers*, as previously raised in the first Office Action, Yoshida invents a method for analyzing a semiconductor die (2, 3) having silicon-on-insulator (SOI) structure 1s and a back side opposite circuitry 1f & 1g near a circuit side, as shown in Fig.1, the method comprising:

- removing substrate 1a shown in Fig.1 from the back side of the semiconductor die and exposing a region 1c of the insulator of the SOI structure, as recited in Col.5/ll.8-13; and
- inducing a detectable response from the exposed region as a function of a portion of the circuitry, as recited in Col.5/ll.19-32, and therefrom, analyzing the die, as recited in Col.5/ll.52-60.

This ground of rejection is the same as previously made in the 2nd Office Action.

24. Regarding claim 2, Yoshida's method of inducing response is by using an electron beam 15 (EB) shown in Fig.2, as recited in Col.5/ll.19-32 & Col.5/ll.53-55.

25. Regarding claim 8, Yoshida's detectable response is obtained from source/drain region 1e (S/D = diffusion region) shown in Fig.1 and Fig.5, as disclosed in Col.5/ll.1-5.

As previously explained in section 17, a detectable signal is still obtained even if no secondary electron is emitted, eventually because layer 1c in Fig.5 has been removed (see also next rejection of claim 9).

26. Regarding claim 9, the step of using the BOX layer 1c in Fig.1 and Fig.5 as a dielectric in inducing a detectable response is disclosed in Col.6/ll.51-56, i.e., from the absence of secondary electrons thereby detected (from 1st Office Action), and further, in Col.5/ll.55-63, in the form of potential waveform and contrast image shown in Fig.3 (from 2nd Office Action), more specifically in Col.6, lines 14 & 52, as recited in the previous Response to Applicant's Arguments, section 14.

27. Regarding claim 10, the step of removing a portion of the substrate 1a to expose a portion of the BOX 1c, as shown in Fig.1 and recited in Col.5/ll.8-32.

28. Regarding claim 11, Yoshida's method is a post-manufacturing analysis because the device is analyzed after its manufacture is completed, as recited in Col.6/ll.14-19.

29. Claims 16 and 17 are apparatus (system) claims reciting limitations that are already rejected in claim 1. The additional recitation of a detector in claim 17 is shown by Yoshida as numeral 14 in Fig.2 (from 1st Office Action), and is also inherent in Col.5/ll.56-60 (from 2nd Office Action).

30. Regarding claims 18 and 19, the limitation of using a controller to control the substrate removal in claim 17 is rendered obvious by Yoshida's use of the SOI layer as an etching stop to control the substrate removal process, as recited in Col.6/ll.58-60.

This rejection applies in the event that Applicant interprets the "insulator of SOI structure" recited in claims 1 and 2 as a BOX layer, as previously applied in the second Office Action.

31. Still regarding claims 18 and 19, the limitation of using a controller to control the substrate removal in claim 17 is rendered obvious by Yoshida's use of the BOX layer as an etching stop to control the substrate removal process, as recited in Col.5/ll.33-41, specifically in Col.5/line 39.

This rejection applies in the event that Applicant interprets the "insulator of SOI structure" recited in claims 1 and 2 *as the insulator layer beneath the gate between the S & D layers*, as previously applied in the first Office Action.

32. (Claim 20 has been cancelled)

33. Claims 3-7, 12-13 and 21-23 stand rejected under 35 U.S.C. 102(a) and 102(e) as being *anticipated* by Yoshida. Note: Claim 14 is now rejected *only* under its previously alternative § 103(a) rejection.

34. Regarding claim 3, the step of detecting secondary electrons in response to the EB 15 and the portion of the circuitry is recited in Col.5/ll.19-22, whereas the use of a scanning electron microscope (SEM) is inherent in Yoshida's, as detailed in the above Response to Applicant's Arguments. The previously recited supporting prior arts are now used in an additional rejection of claim 3 under § 103(a).

35. Regarding claim 4, the step of analyzing the die by detecting the difference between the secondary electron signals obtained from two selected circuit portions is shown by the device 1X in Fig.3, which consists of a plurality of circuit portions (1s & 1f) shown in Fig.5, which represents voltage variations across the plurality of circuit portions, results in a waveform shown in Fig.3, as recited in Col.6/ll.7-11.

This rejection applies in the event that Applicant interprets the "insulator of SOI structure" recited in claims 1 and 2 as a BOX layer, as previously applied in the second Office Action.

36. Still regarding claim 4, the step of analyzing the die by detecting the difference between the secondary electron signals obtained from two selected circuit portions is shown by the device 1X in Fig.3, which consists of a plurality of circuit portions (1s & 1f) of Fig.1, which represents voltage variations across the plurality of circuit portions, resulting in a waveform shown in Fig.3, as recited in Col.5/ll.53-67.

This rejection applies in the event that Applicant interprets the "insulator of SOI structure" recited in claims 1 and 2 *as the insulator layer beneath the gate between the S & D layers*, as previously applied in the first Office Action.

37. Regarding claims 5 and 21, the step of obtaining an image of the die that represents variations in voltage across the plurality of circuit portions is recited in Col.5/ll.57-63, and shown in Fig.3 and Fig.4.

This rejection applies in the event that Applicant interprets the "insulator of SOI structure" recited in claims 1 and 2 as a BOX layer, as previously applied in the second Office Action.

38. Still regarding claims 5 and 21, the step of obtaining an image of the die that represents variations in voltage across the plurality of circuit portions is recited in Col.5/ll.57- 67 and Col.6/ll.1-6, as shown in Fig.3 and Fig.4.

This rejection applies in the event that Applicant interprets the "insulator of SOI structure" recited in claims 1 and 2 *as the insulator layer beneath the gate between the S & D layers*, as previously applied in the first Office Action.

39. Regarding claim 6, the step of using a pulsed EB is disclosed in Col.6/ll.1-6.

40. Regarding claim 7, the step of using a coupling power supply and inputting electrical signals to the die to generate a response is inherent in Yoshida's, as implicated by the testing set 11 shown in Fig.2, recited in Col.5/ll.53-60, which inherently and conventionally includes a power supply. (See the above Response to Applicant's Argument, section 10).

41. Regarding claim 12, the electrical stimulus applied to the circuitry in the die is provided by the DUT board 12 shown in Fig.2, recited in Col.2/ll.1-4 and Col.5/ll.43-48.

42. Regarding claim 13, to stimulate a response by using the DUT board 12, until a failure is induced in the die, is a mere matter of deliberate choice, which is inherent in the use of Yoshida's DUT, as meticulously elucidated in the above Response to

Applicant's Arguments. In the present Office Action, claim 13 is *additionally* rejected under a § 103(a) rejection.

43. Regarding claim 22, the limitation that the image of the die shows light and dark areas, the dark areas being indicative of circuit portions having positive voltage greater that that of the lighter areas, is recited by Yoshida in Col.6/ll.1-4.

44. Regarding claim 23, the step of using a tester adapter to introduce electrical stimulus to the die is disclosed in testing set 11 shown in Fig.2, as recited Col.5/ll.53-60.

Claim Rejections - 35 USC § 103

45. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

46. In ***addition*** to the above §102 rejection, claim 13 is ***also*** rejected under 103 (a) as being obvious over Yoshida.

Yoshida shows all the limitations of claim 13, as previously applied to claims 1, 11 and 12, although the step of "*inputting a signal (through the DUT board 12)* ***known*** *to induce a failure in the die*" is not explicitly recited, since such a step is inherent in a conventional use of Yoshida's DUT board, as already brought up in the previous §102 rejection of claim 13, ***and*** is also generally known to one of ordinary skill in the art, as

evidenced by the Examiner's example of a 10 kV pulse, which is *known*, with guarantee, to induce a failure in the die.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to *input a signal (through the DUT board 12)* ***known*** *to induce a failure in the die* (e.g., a 10 kV signal) in order to produce a damaged circuit that can be used for comparison, i.e., to distinguish between a functioning die/circuitry and a defective and non-functioning or failing die/circuitry.

However, one of ordinary skill in the art, ***would not*** apply 10 kV or 100 kV pulse just to damage the die for no purpose, since such action would be completely senseless (nonsense). It would have more sense to apply a signal and vary it sofar, ***until*** a failure is induced in the die, which is a more meaningful step already recited by the Examiner in both previous Office Actions.

As ***already recited in both previous Office Actions***, all the alternative/optional steps and motivations recited above are mere matter of deliberate choice, given a device such as Yoshida's DUT board 12.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to *input a signal through the DUT board 12* ***until*** *a failure is induced in the die*, since it is conventional and desirable in the semiconductor industry to test a device for its maximum ratings, and it is also conventional to have such ratings in a manufacturer's data sheet.

This 103 rejection is an *additional* rejection to the above 102 rejection of claim 13, the latter being the same as what has been previously applied in both previous Office Actions, and hence, does not represent a new ground of rejection.

47. Claim 14 *stands* rejected under 103 (a) as being obvious over Yoshida.

Yoshida shows all the limitations of claim 14, as previously applied to claims 1, 11 and 12, except the limitation of inputting the signals in a continuous loop.

This limitation is basically an automation of a step, or method, which is normally implemented manually. It would have been obvious to one having ordinary skill in the art at the time the invention was made to put the input signals in a continuous loop, since it has been held that broadly providing a mechanical or automatic means to replace manual activity which has accomplished the same result involves only routine skill in the art. *In re Venner*, 120 USPQ 192.

One would have been motivated to make the testing steps automatic, since such automation brings significant savings in work and time.

This 103 (a) rejection has been already applied in both previous Office Actions, and hence, does not represent a new ground of rejection.

48. New claims 24 - 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida.

Regarding claim 24, Yoshida invents a method for analyzing a semiconductor die (2, 3) having silicon-on-insulator (SOI) structure 1s and a back side opposite circuitry 1f & 1g near a circuit side, as shown in Fig.1 and Fig.5, irrespective of whether Applicant

interprets the "insulator of SOI structure" recited in claim 24 as a BOX layer, or, *as the insulator layer beneath the gate between the S & D layers*, the method comprising:

- removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed, which is the same as the corresponding limitation of previously rejected claims 1 & 16;
- inputting electrical signals to the die to operate the die in a continuous loop known to cause a failure in a portion of the circuitry in the die, which is the same as the limitations of claims 13 & 14; and
- directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing and therefrom analyzing the die, which is the same as the limitations of claims 1, 2, 13 and 14, wherein the knowledge of the characteristics of a die with failing circuitry is specifically obtained from a step according to previously rejected claim 13.

Therefore, claims 24 is rejected under the same ground(s) and prior art(s) as previously applied to rejected claims 1, 2, 13 and 14, i.e., as being obvious over Yoshida.

► Specifically regarding claim 25, the limitation of detecting a change in secondary electrons emitted from the exposed region of the insulator -- whereby the change is obtained from comparing a functioning die/circuitry to a failing die/circuitry -- is practically the same as that of claim 13. Therefore, claims 25 is also rejected under the same ground(s) and prior art(s) as the rejected claims 1, 2, 13 and 14, i.e., as being obvious over Yoshida.

► Specifically regarding claims 26 and 27, the limitation of detecting a failure of the die in response to detecting an *uninhibited* or *inhibited* emission of secondary electrons is well known in the art to directly depends very much on whether the failure is a short circuit or an open circuit, thus, also depends on whether the portion being analyzed is on a (digitally) high voltage (HI) or a low voltage (LO), the two conditions being distinguishable from the emitted secondary electrons, whereby a "black" (secondary electron emission inhibited) indicates a HI condition, whereas a "white" (secondary electron emission uninhibited) indicates a LO condition, as depicted in Fig.4 and recited in Col.6/ll.1-6.

49. Insofar as the Examiner can ascertain beyond the previous § 112 rejections, the limitation of (detecting) logic states of a plurality of circuit nodes in a die, is rendered obvious by Yoshida in Col.6/ll.11-14 according to a method recited in Col.6/ll.1-6 applied previously, beyond which the limitations of claim 28 are essentially the same as those of previously rejected claim 24, whereas the limitations of claim 29 are essentially the same as those of previously rejected claims 26 and 27. Therefore, claims 28 & 29 are rejected for the same reasons and over the same prior art(s) as previously rejected claims 14, 26 and 27.

50. ***In addition*** *to the previous* 35 U.S.C. 102(a) and (e) rejections, which remain the same as previously applied in the first and second Office Actions, claim 3 *is now* ***also*** rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida.

Yoshida shows all the limitations of claim 3, as previously applied to the § 102 rejections of claims 1 &2, although the word SEM (secondary electron microscope) is *not explicitly* recited. As described in the above Response to Applicant's Arguments, section 9, an SEM is inherent in Yoshida's, as recited in Col.5/ll.42-46, Col.5/ll.53-60 and Col.6/ll.7-11, referring to Fig.2 and Fig.13, wherein the EB source 13, the EB 13, the sample 1X, secondary electrons 16 and secondary detector 14, in combination with Yoshida's claims 2, 6, 8 and 10, altogether form effectively a secondary electron microscope (SEM) recited in Applicant's claim 3. This is an Official Notice supported by many published documents, including Talbot et al. (USPAT #6,091,249) as recited in Col.3/ll.13-16 & Col.6/ll.59-60, as well as by Steffan et al. (USPAT #6,200,823 B1), as recited in Col.1/ll.64-67.

51 Claim 15 *stands* rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al. (USPAT #6,019,249) and Steffan et al. (USPAT #6,200,823 B1).

Yoshida shows all the limitations of claim 15 (previous misprint), as previously applied to the parent claim 1, except the recitation of using a non-defective die as a reference. Talbot et al. disclose a method for analyzing a semiconductor die using an electron beam from a SEM 20 shown in Fig.1, as recited in Col.5/ll.33-57. Talbot's apparatus and method use a defect-free device as reference, as recited in Col.6/ll.65-67.

It would have been obvious to adopt Talbot's use of a non-defective die as a reference in Yoshida's method, since from a single image of a device alone *in the absence of other information*, it is difficult to determine whether or not the device under testing (DUT) contains an error, as implicated by Talbot et al. in Col.6/ll.63-65.

One would have been motivated to compare the EB image of a DUT with a known, non-defective device, as used by Talbot et al., since a defective die would be much more easily and much more quickly recognized by an operator, especially when the image of the non-defective die is subtracted from the currently measured image of a DUT (die under testing), thus highlighting the defect, as suggested by Steffan et al. in Col.3/ll.8-13.

FINAL REJECTION

52. Applicant's New Claims necessitated the new ground(s) of rejection presented in this Office Action, whereas all previously existing claims (1-19 and 21-23) stand under the same grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

53. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bernard E Souw whose telephone number is 703 305 0149. The examiner can normally be reached on Monday thru Friday, 9:00 am to 5:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John R Lee can be reached on 703 308 4116. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872 9318 for regular communications and 703 872 9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

bes
April 26, 2003

JOHN R. LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800